REMARKS

Claims 38-57 were previously pending in this application. Claims 38, 45, and 49 have been amended. As a result, claims 38-57 are pending for examination with claims 38 and 52 being independent claims. No new matter has been added.

Objections to Specification

The title was objected to as not being descriptive. In response, Applicant has amended the title to reflect the invention to which the claims are directed, and respectfully requests that the objection be withdrawn.

The specification was objected to as the specification includes references to related applications that are not updated. In response, Applicant reviewed the specification and has updated all references to related applications. Applicant therefore respectfully requests that the objection be withdrawn.

The summary was objected to as not being proper under 37 C.F.R. 1.73. In particular, the Examiner objected to the use of legal language and phraseology. In response, Applicant has amended the summary to remove the legal language and phraseology and respectfully requests that the objection be withdrawn.

Non-Art Claim Rejections

Claims 38-51 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. In response, Applicant has amended claims 38, 45, and 49 to be more clear, and respectfully requests that the rejection be withdrawn. More particularly, Applicant has amended claims 45 and 49 to remove the antecedent basis problems identified therein, and has amended claim 38 to specify that the subsequent instruction and new instructions are fetched from "respective locations" instead of "the target location."

Double Patenting Rejection

The claims 38-57 were rejected under the judicially-created doctrine of obviousness-type double patenting as being unpatentable over claims 1-27 of U.S. Patent No. 5,961,637.

Submitted herewith is a Terminal Disclaimer with respect to U.S. Patent No. 5,961,637, and therefore the obviousness-type double patenting rejection should be withdrawn.

Allowable Subject Matter

Claims 50-51 were indicated as being allowable if written in independent form. As discussed further below, Applicant believes the independent claims are allowable over the art of record and therefore claims 50 and 51 have not been rewritten in independent form as they are allowable for at least the same reasons as the claims from which they depend.

Art Rejections

Claims 38-42, 44-46, 48-49, and 52-53 were rejected under 35 U.S.C. §102(b) as being anticipated by Bruckert, et al., (U.S. Patent No. 4,742,451, hereinafter "Bruckert"). Applicant respectfully traverses this rejection.

Bruckert teaches a digital processing system that processes prefetched instructions including a conditional branch instruction (Abstract). The processor includes a fetch unit that has separate portions, one that retrieves operands and the other that retrieves instructions (Abstract). When the fetch unit fetches a conditional branch instruction, it may continue to prefetch "branch not taken" instructions using the instruction fetch portion (Abstract). The fetch unit initially uses the operand fetch portion to prefetch "branch taken" instruction. If it is determined that the branch is not take, the prefetch operation is aborted, otherwise the prefetch operation is allowed to continue to provide the next instruction used by the processor (Abstract).

More particularly, the fetch unit is divided into two sections, or "ports", one of which fetches instructions from the memory (Col. 2, lines 49-51). The second section fetches operands from the memory (Col. 2, lines 51-52). In response to a conditional branch instruction, the fetch unit determines the address of the "branch taken" instruction stream, and uses the operand fetch portion to begin prefetching instruction words from the "branch taken" instruction stream (Col. 2, lines 52-56).

More particularly, fetch unit 30 includes two portions, one of which decodes the operand specifiers, fetches the operands from and stores processed data in memory unit 11 (Col. 7, lines 17-20). This portion includes virtual address latch 57, arithmetic and logic unit 56, multiplexers

55, 64 and 65, registers 54, buffers 50 and 63, and instruction decoder 51 (Col. 7, lines 20-23). The second portion of the fetch unit retrieves instruction words from memory unit 11 (Col. 7, lines 23-24). This portion includes VIBA virtual instruction buffer address latch 70, multiplexer 72 and arithmetic and logic unit 71 (Col. 7, lines 24-27). When the instruction decoder 51 decodes a conditional branch instruction, fetch unit 30 uses the operand decode and fetch portion, specifically virtual address latch 57, multiplexer 65, and arithmetic and logic unit 56, to initiate a prefetch of the "branch taken" instruction stream (Col. 7, lines 28-33). In summary, Bruckert includes a single fetch unit, portions of which may be configured to alternately retrieve branch taken and branch not taken instructions.

By contract, independent claim 38 recites a computer system for fetching, decoding and executing instructions comprising storage circuitry for holding a plurality of instructions at respective storage locations, instruction fetch circuitry for fetching instructions from said storage circuitry, the instruction fetch circuitry including an indicator for providing an indication of a next address at which a next fetch operation is to be effected and a first and second instruction fetcher for fetching, respectively, a subsequent instruction and a new instruction, and execution circuitry for executing fetched instructions comprising a branch instruction indicating a target location from which the subsequent instruction may be fetched, wherein said instruction fetch circuitry is operated responsive to execution of said branch instruction to fetch in parallel the subsequent instruction and the new instruction from said respective locations.

Bruckert does not anticipate claim 38. In particular, Bruckert does not disclose "instruction fetch circuitry including... a first and second instruction fetcher for fetching, respectively, a subsequent instruction in a new instruction... wherein said instruction fetch circuitry is operated responsive to execution of said branch instruction to fetch in parallel the subsequent instruction and the new instruction from said respective locations," as recited in claim 38. Bruckert includes a single fetcher including a first portion that decodes operand specifiers and fetches operands from a memory unit, and a second portion that retrieves instruction words from the memory unit (Col. 7, lines 17-27). Based upon a determination (by the first portion) of an operand specifier including a displacement value, that, when added to the contents of the program counter, determines the address of the first instruction in the branch taken instruction stream. This address determination results in the transmission of a memory

request to initiate the retrieval of a first instruction in the branch taken instruction stream (Col. 7, lines 34-53). However, Bruckert does not disclose instruction fetch circuitry including a first and second instruction fetcher that fetches in parallel the subsequent instruction and the new instruction from said respective locations, as recited in claim 38. Bruckert only teaches a first portion of a single fetcher that retrieves an operand specifier indicating a displacement value which determines where a branch taken instruction should be fetched. However, Bruckert does teach two fetchers that fetch a subsequent instruction and a new instruction in parallel, as Bruckert is only capable of fetching by the fetch unit 30 one instruction at a time. More particularly, Bruckert only uses the first portion to fetch operands (not instructions) that indicate (along with the program counter) an address to which a branch is taken; Bruckert does not teach two fetchers that fetch subsequent and new instructions in parallel. Therefore, Bruckert does not anticipate claim 38 and the rejection should be withdrawn. Claims 39-51 depend from claim 38 and are allowable for at least the same reasons.

Independent claim 52 recites a method of operating a computer to fetch decode and execute instructions which computer has storage circuitry holding a plurality of instructions at respective storage locations, said plurality of instructions being arranged in instructions strings, each string comprising a first instruction and a set of subsequent instructions the method comprising fetching instructions from said storage circuitry and providing an indication of a next address at which a next fetch operation is to be effected, wherein a first instruction fetcher fetches subsequent instructions and a second instruction fetcher fetches new instructions, decoding said fetched instructions, executing said fetched instructions comprising a branch instruction indicating a target location from which a subsequent instruction may be fetched, the subsequent instruction being from a different instruction string.

Bruckert does not anticipate claim 52. As discussed above with respect to claim 38, Bruckert does not teach two fetchers. Therefore, Bruckert does not disclose "a first instruction fetcher fetches subsequent instructions and a second instruction fetcher fetches new instructions," as recited in claim 52. Therefore, claim 52 distinguishes over Bruckert and the rejection should be withdrawn. Claims 53-57 depend from claim 52 and are allowable for at least the same reasons.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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